REMARKS

Prior to the present amendment, claims 1-3, 6-7, 9-10, 13, 15, and 19 were pending in the present application. By the present amendment, claims 1, 3, 6, 9, 15, and 19 have been amended, claims 2 and 7 have been canceled, and new claim 21 has been added. Thus, claims 1, 3, 6, 9-10, 13, 15, 19, and 21 remain in the present application. Reconsideration and allowance of pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 in view of the above amendments and the following remarks are requested.

A. Rejection of Claims 1-3, 6, 9-10, and 15 under 35 USC §102(b)

The Examiner has rejected claims 1-3, 6, 9-10, and 15 under 35 USC §102(b) as being anticipated by U.S. Patent Number 6,190,975 to Kubo et al. (hereinafter "Kubo"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by amended independent claims 1, 9, and 15, is patentably distinguishable over Kubo.

The present invention, as defined by amended independent claim 1, requires a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel. As disclosed in the present application, in one embodiment of the present invention, FET 102 is situated on substrate 104 and includes gate electrode layer 114, gate dielectric layer 116, and

channel 112, where gate dielectric layer 116 is situated over channel 112 and gate electrode layer 114 is situated over gate dielectric layer 116, and where channel 112 is situated in substrate 104. *See*, e.g., Figure 1 and related text of the present application. As disclosed in the present application, gate dielectric layer 116 can have a thickness of between 10.0 Angstroms and 15.0 Angstroms, for example. *See*, e.g., page 7, lines 1-2 of the present application.

As disclosed in the present application, gate electrode layer 114 and gate dielectric layer 116 can be selected such that gate electrode layer 114 has a coefficient of thermal expansion (CTE) that is higher than a CTE of gate dielectric layer 116, which advantageously increases carrier mobility in channel 112 by creating a tensile strain in the channel. *See*, e.g., page 7, lines 7-9 of the present application. As disclosed in the present application, in an embodiment in which FET 102 is a PFET, gate dielectric layer 116 and gate electrode layer 114 are selected such that gate dielectric layer 116 has a CTE that is higher than a CTE of gate electrode layer 114 so as to create compressive strain in channel 112, which advantageously increases carrier mobility in the channel. *See*, e.g., page 7, lines 13-17 and Figure 1 of the present application.

In contrast to the present invention as defined by amended independent claim 1, Kubo does not disclose a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel. Instead of a

complimentary semiconductor device (CMOS device) formed on a silicon structure, Kubo is directed to a heterostructure CMOS device (referred to as an HCMOS device in Kubo) using Si/SiGe (mixed crystal of the IV-family elements). See, e.g., column 1, lines 26-30 of Kubo.

As disclosed in Kubo, the HCMOS device utilize, as a channel, the interface of a heterojunction structure of two kinds of semiconductors different in band gap from each other, instead of the Si/SiO_2 interface. *See*, e.g., column 1, lines 30-34 of Kubo. Thus, the FET (i.e. the HCMOS device) disclosed in Kubo is substantially different than the FET as specified in amended independent 1. In particular, since the channel in the HCMOS device is formed in a semiconductor layer that is formed over the substrate, the channel is not situated in the substrate. Thus, Kubo fails to disclose a channel situated in a substrate, as specified in amended independent claim 1.

Kubo specifically discloses an HCMOS device including NMOS and PMOS transistors situated on silicon substrate 10. *See*, e.g., Figure 1 and related text of Kubo. In Kubo, the NMOS transistor has a substantially similar structure as the PMOS transistor and includes gate electrode 18n, gate insulating layer 19n, Si layer 17n, SiGe layer 15n, and SiGeC layer 14, where a carrier accumulation layer formed in the vicinity of the interface at the side of SiGeC layer 14n serves as a channel in which electrons travel at a high speed. *See*, e.g., column 9, lines 1-6 and lines 24-25 and Figure 1 and related text of Kubo. Thus, in Kubo, SiGeC layer 14n serves as the channel for the NMOS transistor.

However, in Kubo, p-well 11 (a high-concentration p-type silicon layer) is formed on silicon substrate 10, Si layer 13n is formed on p-well 11, a spacer layer is formed on Si layer 13n, and SiGeC layer 14n is formed on the spacer layer. *See*, e.g., column 8, lines 51-57 and Figure 1 of Kubo. Thus, in Kubo, since SiGeC layer 14n is not formed in silicon substrate 10, SiGeC layer 14n is not a channel situated in a substrate, as specified in amended independent claim 1. In Kubo, the electron mobility is higher in SiGeC layer 14n than in the Si layer, thus increasing the operational speed of the NMOS transistor. *See*, e.g., column 9, lines 4-6 of Kubo. Kubo discloses that by adjusting the composition rates of Si, Ge, and C in the SiGeC layer (e.g. SiGeC layer 14n), the band gap amount and lattice misfit with respect to silicon can be changed. *See*, e.g., column 10, lines 18-22 of Kubo.

However, Kubo fails to disclose a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel, as specified in amended independent claim 1. In fact, Kubo fails to mention any relationship between a CTE of gate electrode 18n and a CTE of gate insulating layer 19n. Also, gate insulating layer 19n (or gate insulating layer 19p) has a thickness of about 5 nm (i.e. about 50.0 Angstroms). In contrast, the thickness of the gate dielectric as disclosed in the present application and as specified in claims 6, 9, and 21 is between 10.0 Angstroms and 15.0 Angstroms. Thus, the thickness of gate insulating layer 19n

(or gate insulating layer 19p) disclosed in Kubo is substantially thicker (i.e. more than three times as thick) as the gate dielectric as disclosed in the present application and as specified in claims 6, 9, and 21.

In the outstanding Office Action, the Examiner asserts:

> It is noted that the first gate dielectric is made of silicon oxide and the first gate electrode made of polysilicon. Thus, the first coefficient of thermal expansion should be different from the second coefficient of the thermal expansion since the coefficient of thermal expansion depends on the material (See Wolf et al.), and this thermal expansion difference would naturally cause a strain in the channel and thereby increase mobility in said FET. The term "selected to have" is merely the intended use. The difference I the first coefficient of thermal expansion and the second coefficient of thermal expansion inherently causes a strain in the channel and thereby increases carrier mobility in said FET. *See* page 3 of the Office Action dated December 9, 2008.

Applicants do not dispute the teachings of Wolf. However, amended independent claim specifies that the first gate electrode and the first gate dielectric are selected such that the second coefficient of thermal expansion is greater than the first coefficient so as to cause an increase in carrier mobility in the channel. As disclosed in the present application, this is (by implication) true for an NFET. However, as disclosed in the present application, for a PFET, carrier mobility is increased in the channel as a result of a compressive strain in the channel which occurs when the first coefficient of thermal expansion (e.g. the CTE of gate dielectric layer 116) is greater than the second coefficient of thermal expansion (e.g. the CTE of gate electrode layer 114). *See*, e.g., page 7, lines 13-17 of the present application. Thus, to increase carrier mobility in the channel, the required relationship between CTE of the gate electrode and the CTE of the gate dielectric depends on whether the FET is an NFET or a PFET. Applicants submit

that the distinction between the type of strain (i.e. tensile strain or compressive strain) produced in the channel to cause an increase in carrier mobility and the type of FET (i.e. NFET or PFET) is not disclosed in Wolf or Kubo.

For all the foregoing reasons, Applicants respectfully submit that, at the time the invention defined by amended independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kubo. Thus, amended independent claim 1 is patentably distinguishable over Kubo and, as such, claims 3 and 6 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Amended independent claim 9 defines similar subject matter as amended independent claim 1, with a difference being that amended independent claim 9 specifies that the first gate dielectric has a thickness of between 10.0 Angstroms and 15.0 Angstroms. As discussed above, Kubo discloses a gate insulating layer (e.g. gate insulating layer 19n or gate insulating layer 19p) having a thickness of about 5 nm (i.e. about 50.0 Angstroms), which is substantially greater than the gate dielectric thickness as specified in amended independent claim 9. Thus, for all of the reasons discussed above, amended independent claim 9 is also patentably distinguishable over Kubo. As such, claim 10 depending from amended independent claim 9 is also patentably distinguishable over Kubo for at least the reasons presented above and also for the additional limitations contained in the dependent claim.

The present invention, as defined by amended independent claim 15, requires a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said first coefficient of thermal expansion is greater than said second coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel, and where the FET is a PFET. For similar reasons as discussed above, Applicants respectfully submit that, at the time the invention defined by amended independent claim 15 was made, the invention would not have been obvious to a person of ordinary skill in the art by Kubo. As such, amended independent claim 15 is patentably distinguishable over Kubo.

B. Rejection of Claims 7, 13, and 19 under 35 USC §103(a)

The Examiner has rejected claims 7, 13, and 19 under 35 USC §103(a) as being unpatentable over Kubo. As discussed above, amended independent claims 1, 9, and 15 are patentably distinguishable over Kubo. Thus claim 13 depending from amended independent claim 9 and claim 19 depending from amended independent claim 15 are, *a fortiori*, also patentably distinguishable over Kubo for at least the reasons presented above and also for additional limitations contained in each dependent claim.

C. **Conclusion**

For all the foregoing reasons pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 are patentably distinguishable over the cited art, and an early allowance of pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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Respectfully Submitted,
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